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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,074	11/19/2003	Peter Dean Swartz	GENSP052	1073

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EXAMINER	
RICHER, AARON M	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,074	SWARTZ ET AL.	
	Examiner	Art Unit	
	Aaron M. Richer	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20031119*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims are rejected under 35 U.S.C. 102(b) as being anticipated by Gryskiewicz (U.S. Patent 6,392,712).

3. As to claims 1, 12, 14, 23, and 25, Gryskiewicz discloses a configurable real time data processor arranged to provide a display data stream to a display unit having an associated set of display attributes, comprising:

a number of ports each of which is configured to receive an input data stream (fig. 1, elements 120, 130);

a format converter unit coupled to one of the ports arranged to convert a corresponding input data stream to a progressive type data stream, if needed (fig. 1, elements 104, 106, 128, 122);

a number of adaptive image converter units each coupled an associated one of the ports suitable for converting a corresponding input data stream to a corresponding converted data stream having associated converted data stream attributes (fig. 1; converter units to go from interlaced to progressive and progressive to interlaced are both provided);

an image compositor unit arranged to combine the converted data streams to form a composited data stream (fig. 1, element 156);

an image enhancer unit arranged to enhance the composited data stream to form an enhanced data stream (col. 8, lines 19-27; a "flicker" filter is used to enhance one of the streams, which in turn enhances the composited stream);

a display unit interface arranged process the enhanced data stream to form the display data (fig. 1, elements 158, 160);

and a memory unit bi-directionally coupled to each of the image converter units and the image compositor arranged to store selected portions of selected ones of the data streams from the image converter units and to provide the selected portions to the image compositor as needed (fig. 4, FIFO buffers are supplied as memory to store frames until the mixer is ready for them).

4. As to claims 2, 13, and 24, Gryskiewicz discloses a processor comprising: a progressive scan timing generator arranged to provide a progressive scan timing signal to the converter units such that the converted data streams are progressive scan type data streams (fig. 1-2, col. 3, lines 54-65; timing information is provided for progressive conversion).

5. As to claim 3, Gryskiewicz discloses a processor comprising: a de-interlacing unit coupled to the format converter unit arranged to de-interlace an interlaced type video stream as needed (fig. 1, elements 104 and 106 make up a deinterlacing unit that outputs progressive video).

6. As to claims 4, 15, and 26, Gryskiewicz discloses a processor wherein the converter unit further comprises: a frame rate conversion unit arranged to synchronize each converted data stream to a display frame rate (col. 5, lines 63-67; col. 6, lines 1-42).

7. As to claims 5, 16, and 27, Gryskiewicz discloses a processor wherein the display frame rate is locked to a selected frame rate (col. 5, lines 63-67; col. 6, lines 1-42, in this case the frame rate is 30 Hz or 60 fields/second).

8. As to claims 6, 17, and 28, Gryskiewicz discloses a processor wherein the locked frame rate corresponds to one of the incoming data streams (col. 1, lines 6-26; col. 2, lines 54-65; NTSC video, which is also 60 fields/second, is used as an input).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 7, 18, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gryskiewicz in view of Naegle (U.S. Publication 2004/0012577).

11. As to claims 7, 18, and 29, Gryskiewicz does not expressly disclose a processor wherein the display frame rate is a free running frame rate. Naegle, however, does disclose a video processor with a free running frame rate. The motivation for this is to provide a larger set of pixel clock frequencies for various formats (p. 1, paragraph

0014). It would have been obvious to one skilled in the art to modify Gryskiewicz to use a free running frame rate in order to support more diverse formats as taught by Naegle.

12. Claims 8, 9, 19, 20, 30, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gryskiewicz.

13. As to claims 8, 19, and 30, Gryskiewicz discloses a processor wherein the ports include, a video receiver port arranged to receive video data (fig. 1, elements 120 and 130). Gryskiewicz does not expressly disclose a user interface port arranged to receive user input commands and a network interface arranged bi-directionally connected to a network arranged to transceive packet based data to and from the network. However, Gryskiewicz does disclose a set-top box (col. 9, lines 36-45). Official notice has been taken of the fact that cable set-top boxes with user interfaces connected to a network are well-known in the art (see MPEP 2144.03). It would have been obvious to one skilled in the art to modify Gryskiewicz to use a user interface and connect to a network in order to access digital cable services such as on-demand movies.

14. As to claims 9, 20, and 31, Gryskiewicz does not disclose a processor as an integrated circuit. Official notice has been taken of the fact that graphics processors on integrated circuits are well-known in the art (see MPEP 2144.03). It would have been obvious to one skilled in the art to modify Gryskiewicz to use an integrated circuit in order to make the graphics processor smaller and reduce production costs.

15. Claims 10, 11, 21, 22, 32, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gryskiewicz in view of Leyvi (U.S. Publication 2003/0067552).

16. As to claims 10, 21, and 32, Gryskiewicz does not disclose a processor wherein the display attributes are Extended Display Identification Data (EDID). Leyvi, however, discloses a conversion process in which EDID is used. The motivation for this is to easily determine whether a format is compatible with a display (p. 3, paragraph 0025). It would have been obvious to one skilled in the art to modify Gryskiewicz to use EDID in order to determine format compatibility as taught by Leyvi.

17. As to claims 11, 22, and 33, Gryskiewicz discloses a processor that comprises: an interlacer unit arranged to interlace a progressive scan image when the display unit is an interlaced type display unit (fig. 1, element 150). Although Gryskiewicz mentions displaying on a progressive display (col. 1, lines 39-52), the described embodiments of Gryskiewicz deal only with an interlaced display. Therefore, Gryskiewicz does not disclose a progressive scan bypass unit arranged to bypass the interlacer when the display unit is a progressive scan type display unit.

Leyvi, however, discloses a method in which EDID is read to determine whether to bypass a scan converter when a format matches a display (p. 3, paragraph 0025). Leyvi, further discloses that progressive formats are used (p. 1, paragraph 0005). It is logical to then assume that if a signal in progressive format compatible with a display is passed to the invention of Leyvi, conversion will be bypassed. The motivation for this is the same as for any removal of any unnecessary graphics component: to save processing time and power. It would have been obvious to one skilled in the art to modify Gryskiewicz to bypass an unnecessary converter in order to save processing time and power as taught by Leyvi.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron M. Richer whose telephone number is (571) 272-7790. The examiner can normally be reached on weekdays from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on (571) 272-7778. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AMR
6/21/05

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